Remarks

Claims 2 and 8 have been amended. Support for these amendments is found in the specification and drawings, and thus no new matter has been added. Claims 2, 8, 16, and 23 are pending in the present application.

Rejection under § 103

Claims 2 and 8 have been rejected under §103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289) and Susuki et al. (U.S. 5,532,910). In addition, claim 16 has been rejected under § 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098), Distefano (U.S. 6,075,289) and Susuki et al. (U.S. 5,532,910) as applied to claim 2 and further in combination with Corisis et al. (U.S. 2002/0135066).

The Examiner stated that Lo et al. teach all the limitations of independent claims 2 and 8 except, "a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, or a topographic contact." The Examiner also alleged that Distefano discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone of the intermediate substrate and then concluded that it would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to the package of Lo in order to provide thermally enhanced packages as taught by Distefano. The Examiner further alleged that Suzuki et al. utilizes a decoupling capacitor accommodated in a space coupled to a die and concluded that it would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor into the modified package including Lo in order to remove noise as taught by Suzuki et al.

Applicants respectfully traverse these rejections of the claims and submit that the Examiner has not met the burden of establishing a prima facie case of obviousness under §103. MPEP §2145. In order to establish a prima facie case of obviousness under §103, the Examiner has the burden of showing, by reasoning or evidence, that: 1) there is some suggestion or motivation, either in the references themselves or in the knowledge available in the art, to modify

that reference's teachings; 2) there is a reasonable expectation on the part of one of ordinary skill in the art that the modification or combination has a reasonable expectation of success; and 3) the prior art references (or references when combined) teach or suggest all the claim limitations. MPEP §2145. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claims 2 and 8 recite a printed circuit board assembly comprising, *inter alia*, a first semiconductor die, a second semiconductor die, an intermediate substrate positioned between the first semiconductor die and the second semiconductor die, a heat sink including a cap thermally coupled to a major surface at least one of the semiconductor dies, and a decoupling capacitor mounted to a first surface of the substrate, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to a conductive contact on the first surface of the intermediate substrate. Claim 8 further recites that the capacitor is mounted between high and low voltage inputs of the first or second semiconductor dies.

Applicants respectfully submit that none of the references (Lo et al., Distefano, Suzuki et al., or Corisis et al.) teach, suggest, or motivate, singularly or in combination, a decoupling capacitor mounted to the substrate within a stacked chip arrangement, wherein a thickness dimension of the capacitor is accommodated by a space defined by a thickness dimension of a topographic contact conductively coupled to a conductive contact of the substrate. As acknowledged by the Examiner, Lo et al. do not disclose or suggest a decoupling capacitor, let alone a capacitor conductively coupled to one of the first and second semiconductor dies or between high and low voltage inputs, wherein a thickness dimension of the capacitor is accommodated by a space defined by a thickness dimension of a topographic contact conductively coupled to a conductive contact of the substrate. In fact, the only reference applied by the Examiner that does disclose a capacitor is Suzuki et al. (Lo et al., Distefano, and Corisis et al. are all void of any such teaching or suggestion regarding capacitors). However, Suzuki et al. teach the capacitor is mounted on a lead frame so as to be connected in series with the output terminals of a IC chip and sealed in mold resin (22). (Col. 1, lines 48-50). Nowhere does Suzuki et al. teach or suggest, singularly or in combination with Lo et al. or any other reference, a capacitor, wherein its thickness dimension is accommodated by a space defined by a thickness

dimension of a topographic contact that is conductively coupled to a conductive contact of the substrate as recited by Applicants' claims 2 and 8.

To alleviate this deficiency in the prima facie case, the Examiner stated, "With respect to the placement of the capacitor, such that a thickness dimension of said decoupling capacitor accommodated in a space defined by a thickness dimension of one of said first semiconductor, it would have been obvious, since the rearrangements of parts have been held unpatentable absent a showing of criticality or unexpected results." *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950); see also *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975). However, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The **prior art must provide a motivation or reason** for the worker in the art, without the benefit of appellant's specification, **to make the necessary changes** in the reference device." (emphasis added) *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984); see also MPEP §2144.04 (VI)(C). Additionally, the Federal Circuit has stated, "The mere fact that prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritsch*, 23 USPQ2d 1780, 1783-4 (Fed. Cir. 1991).

Applicants respectfully submit that the prior art provides no such motivation or reason. First, the references do not even disclose a capacitor in a stacked arrangement. Second, none of the references teach or suggest, singularly or in combination, a capacitor mounted on a substrate, wherein its thickness is accommodated in a space defined by a thickness dimension of a topographic contact coupled to a conductive contact of the substrate. Third, the prior does not provide a single motivation, suggestion, or reason for one of ordinary skill in the art to make the necessary changes arbitrarily made by the Examiner in the reference device to come up with Applicants' claimed invention. Specifically, placing a decoupling capacitor on a first surface of an intermediate substrate in a space between the substrate and one of the semiconductor dies, wherein the space is defined by a thickness dimension of a topographic contact and accommodates the capacitor. Thus, Applicants believe the Examiner has mistakenly used

Applicants' specification as a "template" to piecemeal the teachings of the prior art to reject Applicants' claims 2 and 8.

Moreover, as set forth above, Suzuki et al.'s capacitor is connected in series to the IC chip's output terminals. In sharp contrast, Applicants' claim 8 recites that the capacitor is coupled between high and low voltage inputs of either the first or second semiconductor die. Applicants respectfully submit that Suzuki et al.'s capacitor connected to output terminals does not teach or suggest the capacitor connected between high and low voltage inputs as recited by Applicants' claim 8. Therefore, Applicants respectfully submit that the none of the references, singularly or in combination, teach or suggest all of the limitations of Applicants' claims 2 and 8.

Finally, with respect to Applicants' independent claim 23, the Examiner rejected claim 23 in the Office Action Summary. See Disposition of Claims, #6. However, the Applicants are unable to find any reasoning or evidence provided by the Examiner in the Detailed Action, starting on page 2, to support this rejection of claim 23. Thus, the Applicants are unsure as to why, and for what reasons, claim 23 was rejected and thus respectfully request this rejection be withdrawn. However, in order to expedite prosecution of this application, Applicants have assumed, *arguendo*, that the Examiner meant to reject Applicants' claim 23 under 35 §U.S.C. 103(a). Applicants' claim 23 recites, in part, that the printed circuit board assembly is configured such that the first and second semiconductor dies span the passage disposed within the intermediate substrate. Lo's first semiconductor chip 26 spans the passage 24, but as shown in Figure 1, neither of the second semiconductor chips (40 or 42) span the passage 24 as recited in Applicants' claim 23. In addition, none of the other references disclose or suggest, singularly or in combination, both dies, a first semiconductor die and a second semiconductor die, spanning a passage within an intermediate substrate of a printed circuit board assembly. Thus, Applicants respectfully submit that none of the references, singularly or in combination, teach or suggest all of the limitations of Applicants' claim 23.

Therefore, the required burden of a prima facie case of obviousness has not been met and the Applicants respectfully request that the rejections under 35 U.S.C. §103 of independent claims 2, 8, and 23 be withdrawn. As claim 16 depends from independent claim 2, the rejection of claim 16 under 35 U.S.C. §103 should be withdrawn as well. Accordingly, the Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve

efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,
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